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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,506	05/11/2004	Liang-Chen Chien	5900/0146PUS1	3505
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Muncy, Geissler, Olds & Lowe, PLLC P.O. BOX 1364 FAIRFAX, VA 22038-1364				PIZIALI, JEFFREY J
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,506	CHIEN ET AL.	
	Examiner	Art Unit	
	JEFF PIZIALI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 October 2009.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 13-23 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 13-23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 07 October 2009 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *7 October 2009* has been entered.

Drawings

2. The drawings were received on *7 October 2009*. These drawings are acceptable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. *Claims 13-23* are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 13 recites the limitations "*the frame data*" (line 11) and "*the present frame data*" (line 14). There is insufficient antecedent basis for these limitations in the claim.

The Applicant is respectfully requested to clarify whether each of these limitations is intended to be identical to, common to, or distinct from the earlier recited "*a plurality of frame data*" (line 9) and/or "*a plurality of delayed frame data*" (line 10).

6. Claim 13 recites the limitation "*the liquid crystal element*" (line 16). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether this limitation is intended to be identical to, or distinct from the earlier recited "*a liquid crystal element*" (line 5) and/or "*a liquid crystal element*" (line 7).

7. Claim 13 recites the limitation "*the voltage value of the frame data in the present frame period... that of the frame data in the previous frame period*" (lines 20-21). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether or not the frame data must have voltage values.

8. Claim 17 recites the limitations "*the frame data*" (line 11) and "*the present frame data*" (line 18). There is insufficient antecedent basis for these limitations in the claim.

The Applicant is respectfully requested to clarify whether each of these limitations is intended to be identical to, common to, or distinct from the earlier recited "*a plurality of frame data*" (line 9) and/or "*a plurality of delayed frame data*" (line 10).

9. Claim 17 recites the limitation "***the liquid crystal element***" (line 20). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether this limitation is intended to be identical to, or distinct from the earlier recited "***a liquid crystal element***" (line 5) and/or "***a liquid crystal element***" (line 7).

10. Claim 23 recites the limitation "***the voltage value of the frame data in the present frame period... that of the frame data in the previous frame period***" (lines 2-3). There is insufficient antecedent basis for this limitation in the claim.

The Applicant is respectfully requested to clarify whether or not the frame data must have voltage values.

11. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

12. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. *Claims 13-16* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Jinda et al (US 2002/0044115 A1)*** in view of ***Ham et al (US 2004/0119730 A1)***.

Regarding claim 13, **Jinda** discloses a method for driving a liquid crystal display panel [e.g., Fig. 8: 15], the method comprising:

receiving a plurality of frame data [e.g., Fig. 8: "input image signal"];
delaying [e.g., Fig. 8: via 11, 12, 13, 14; wherein the frame memories and arithmetic unit inherently delay image signal transmission to the LCD] the frame data to produce a plurality of delayed frame data [e.g., Fig. 4: data value of previous image signal] corresponding to the frame data;

producing an over-drive data voltage pulse [e.g., Fig. 4: matrix of correction values; Fig. 9: b_1] and an original data voltage pulse [e.g., Fig. 4: data value of current image signal; Fig. 9: b_2] according to the present frame data in every frame period; and

sequentially providing the over-drive data voltage pulse [e.g., Fig. 9: b_1] and the original data voltage pulse [e.g., Fig. 9: b_2] to the liquid crystal element of each pixel in a frame period [e.g., Fig. 9: one vertical synchronization interval]; wherein

the voltage value of the over-drive data voltage pulse [e.g., Fig. 4: matrix of correction values; Fig. 9: "high intensity" b_1 during the illustrated one vertical synchronization interval] is decided by comparing a delayed frame data in a previous frame period [e.g., Fig. 4: data value of previous image signal; Fig. 9: "low intensity" value prior to the one vertical synchronization interval] with a frame data in a present frame period [e.g., Fig. 4: data value of current image signal; Fig. 9: "middle intensity" b_2 during the illustrated one vertical synchronization interval] next to the previous frame period, where

if the voltage value of the frame data in the present frame period is larger than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is larger than that of the frame data in the present frame period (*see Paragraph 40, Lines 1-7*);

if the voltage value of the frame data in the present frame period is smaller than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is smaller than that of the frame data in the present frame period (*see Paragraph 40, Lines 7-11*);

if the voltage value of the frame data in the present frame period is equal to that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is equal to that of the frame data in the present frame period (*see Paragraph 40, Lines 11-15*)

(*see the entire document, including Paragraphs 36-59*).

Jinda does not expressly teach the structural details of the liquid crystal panel.

However, **Ham** does disclose a liquid crystal display panel [*e.g., Fig. 5*] comprising:

a plurality of scan lines [*e.g., Fig. 5: 56*];

a plurality of data lines [*e.g., Fig. 5: 55*]; and

a plurality of pixels, each pixel has

a switching device [*e.g., Fig. 5: TFT*] and

a liquid crystal element [*e.g., Fig. 5: Clc*], and

the switching device is connected to a corresponding one of said scan lines,

a corresponding one of said data lines and

a liquid crystal element [e.g., *Fig. 5: Clc*]

(*see the entire document, including Paragraphs 53-63*).

Jinda and **Ham** are analogous art, because they are from the shared inventive field of driving liquid crystal display devices via over-drive pulses.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Ham's** liquid crystal display panel in the place of **Jinda's** LCD panel, so as to make use of an active matrix LCD structure suitable for displaying moving images (e.g., *see Ham: Page 1, Paragraph 5*).

Regarding claim 14, **Jinda** discloses when comparing the present frame data with the corresponding delayed frame data,

the voltage value of the over-drive data voltage pulse is decided according to a table [*Fig. 4: look-up table; Fig. 8: 14*] (*see the entire document, including Paragraphs 38-40*).

Regarding claim 15, **Jinda** discloses each frame data comprises a plurality of pixel data and each pixel data corresponds to a pixel of said pixels (*see the entire document, including Paragraphs 38-40*).

Regarding claim 16, **Jinda** discloses enabling the over-drive data voltage pulse and the original data voltage pulse to be supplied to the liquid crystal display's elements (*see the entire document, including Paragraphs 53-58*).

Moreover, **Ham** discloses providing a scan voltage to the switching device of a pixel of said pixels via the corresponding scan line to enable data voltage pulses to be supplied to the liquid crystal element (*see the entire document, including Fig. 5; Paragraphs 53-63*).

16. *Claims 17-23* are rejected under 35 U.S.C. 103(a) as being unpatentable over **Jinda et al (US 2002/0044115 A1)** in view of **Ham et al (US 2004/0119730 A1)** and **Songer (US 5,844,619 A)**.

Regarding claim 17, **Jinda** discloses a method for driving a liquid crystal display panel [e.g., Fig. 8: 15], the method comprising:

receiving a clock signal [e.g., Fig. 2: "A, B, C,... Y, Z" *write operation signals*],
a synchronization signal [e.g., Fig. 9; *signal providing "one vertical synchronization interval"*], and
a plurality of frame data [e.g., Fig. 8: "*input image signal*"];
delaying the frame data [e.g., Fig. 8: *via 11, 12, 13, 14; wherein the frame memories and arithmetic unit inherently delay image signal transmission to the LCD*] to produce a plurality of delayed frame data [e.g., Fig. 4: *data value of previous image signal*] corresponding to the frame data;

producing a double-frequency clock signal [e.g., Fig. 3: "A, B, C,... Y, Z" *read operation signals*] which has twice the frequency of the clock signal, and

producing a double-frequency synchronization signal [e.g., Fig. 9; "b₁" and "b₂" are applied in half "vertical synchronization intervals"] which has twice the frequency of the synchronization signal;

producing at least an over-drive data voltage pulse [e.g., Fig. 4: matrix of correction values; Fig. 9: b₁] and

an original data voltage pulse [e.g., Fig. 4: data value of current image signal; Fig. 9: b₂] according to the present frame data in every frame period; and

sequentially providing the over-drive data voltage pulse [e.g., Fig. 9: b₁] and the original data voltage pulse [e.g., Fig. 9: b₂] to the liquid crystal element of a corresponding pixel of said pixels in accordance with the double-frequency clock signal in a frame period; wherein

the voltage value of the over-drive data voltage pulse is decided [e.g., Fig. 4: matrix of correction values; Fig. 9: "high intensity" b₁ during the illustrated one vertical synchronization interval] by comparing a delayed frame data in a previous frame period [e.g., Fig. 4: data value of previous image signal; Fig. 9: "low intensity" value prior to the one vertical synchronization interval] with a frame data in a present frame period next to the previous frame period [e.g., Fig. 4: data value of current image signal; Fig. 9: "middle intensity" b₂ during the illustrated one vertical synchronization interval]

(see the entire document, including Paragraphs 36-59).

Jinda does not expressly teach the structural details of the liquid crystal panel.

However, **Ham** does disclose a liquid crystal display panel [e.g., Fig. 8: 15] comprising:

a plurality of scan lines [e.g., *Fig. 5: 56*];
a plurality of data lines [e.g., *Fig. 5: 55*]; and
a plurality of pixels, each pixel includes
a switching device [e.g., *Fig. 5: TFT*] and
a liquid crystal element [e.g., *Fig. 5: Clc*],
the switching device is connected to a corresponding one of said scan lines,
a corresponding one of said data lines and
a liquid crystal element [e.g., *Fig. 5: Clc*]
(see the entire document, including Paragraphs 53-63).

Jinda and **Ham** are analogous art, because they are from the shared inventive field of driving liquid crystal display devices via over-drive pulses.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Ham's** liquid crystal display panel in the place of **Jinda's** LCD panel, so as to make use of an active matrix LCD structure suitable for displaying moving images (e.g., see **Ham: Page 1, Paragraph 5**).

Should it be shown that neither **Jinda** nor **Ham** disclose the instantly claimed clock doubling subject matter with sufficient specificity:

Songer discloses a method for driving a display with a vertical and horizontal synchronized clock doubler [e.g., *Fig. 6: 77*], the method comprising:

receiving a clock signal,
a synchronization signal, and
a plurality of frame data;
producing a double-frequency clock signal which has twice the frequency of the clock signal, and
producing a double-frequency synchronization signal which has twice the frequency of the synchronization signal

(see the entire document, including Column 13, Line 10 - Column 14, Line 45).

Jinda, **Ham**, and **Songer** are analogous art, because they are from the shared inventive field of methods for driving display devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Songer's** vertical and horizontal synchronized clock doubling techniques with **Ham's** and **Jinda's** combined LCD panel, so as to provide significant improvements in resolution, brightness, contrast ratio, and color saturation in the resulting image (e.g., see **Songer**: Column 14, Lines 15-21).

Regarding claim 18, **Jinda** discloses when comparing the present frame data with the corresponding delayed frame data,

the voltage value of the over-drive data voltage pulse is decided according to a table [Fig. 4: look-up table; Fig. 8: 14] (see the entire document, including Paragraphs 38-40).

Regarding claim 19, **Songer** discloses the synchronization signal includes a horizontal synchronization signal and

a vertical synchronization signal (*see the entire document, including Column 13, Line 10 - Column 14, Line 45*).

Regarding claim 20, **Songer** discloses the double-frequency synchronization signal includes a horizontal double-frequency synchronization signal and

a vertical double-frequency synchronization signal (*see the entire document, including Column 13, Line 10 - Column 14, Line 45*).

Regarding claim 21, **Jinda** discloses each frame data comprises a plurality of pixel data and

each pixel data corresponds to a pixel of said pixels (*see the entire document, including Paragraphs 38-40*).

Regarding claim 22, **Jinda** discloses enabling the over-drive data voltage pulse and the original data voltage pulse to be supplied to the liquid crystal display's elements (*see the entire document, including Paragraphs 53-58*).

Moreover, **Ham** discloses providing a scan voltage to the switching device of a pixel of said pixels via the corresponding scan line to enable data voltage pulses to be supplied to the liquid crystal element (*see the entire document, including Fig. 5; Paragraphs 53-63*).

Regarding claim 23, **Jinda** discloses the voltage value of the over-drive data voltage pulse is decided as following:

if the voltage value of the frame data in the present frame period is larger than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is larger than that of the frame data in the present frame period (*see Paragraph 40, Lines 1-7*);

if the voltage value of the frame data in the present frame period is smaller than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is smaller than that of the frame data in the present frame period (*see Paragraph 40, Lines 7-11*);

if the voltage value of the frame data in the present frame period is equal to that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is equal to that of the frame data in the present frame period (*see Paragraph 40, Lines 11-15*).

Response to Arguments

17. Applicant's arguments filed on *7 October 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*As disclosed in claim 13 of the present application, the technical feature, 'delaying the frame data to produce a plurality of delayed frame data*

*corresponding to the frame data' is neither taught nor suggested by **Jinda**"* (see Page 9 of the Response filed on 7 October 2009). However, the examiner respectfully disagrees.

Jinda discloses a method for driving a liquid crystal display panel [e.g., Fig. 8: 15], the method comprising: receiving a plurality of frame data [e.g., Fig. 8: "input image signal"]; delaying [e.g., Fig. 8: via 11, 12, 13, 14; wherein the frame memories and arithmetic unit inherently delay image signal transmission to the LCD] the frame data to produce a plurality of delayed frame data [e.g., Fig. 4: data value of previous image signal] corresponding to the frame data (see the entire document, including Paragraphs 36-59).

Jinda teaches, "*the same image data as the image data outputted from the first FIFO memory 21 is outputted from the second FIFO memory 22 with a delay of one image period*" (see Paragraph 57)

The Applicant contends, "*The way of comparing a delayed frame data in a previous frame period with a frame data in a present frame period next to the previous frame period in order to decide the voltage value of the over-drive data voltage pulse as described in claim 13 of the present invention is neither taught nor suggested by the prior art of **Jinda**"* (see Page 9 of the Response filed on 7 October 2009). However, the examiner respectfully disagrees.

Jinda discloses the voltage value of the over-drive data voltage pulse [e.g., Fig. 4: matrix of correction values; Fig. 9: "high intensity" b₁ during the illustrated one vertical

synchronization interval] is decided by comparing a delayed frame data in a previous frame period [e.g., Fig. 4: *data value of previous image signal*; Fig. 9: "low intensity" value prior to the one vertical synchronization interval] with a frame data in a present frame period [e.g., Fig. 4: *data value of current image signal*; Fig. 9: "middle intensity" b_2 during the illustrated one vertical synchronization interval] next to the previous frame period (see the entire document, including Paragraphs 36-59).

The Applicant contends, "the prior art of *Jinda* fails to teach the way Of determining an over-drive data value as adopted in the present invention" (see Page 9 of the Response filed on 7 October 2009). However, the examiner respectfully disagrees.

Jinda discloses if the voltage value of the frame data in the present frame period is larger than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is larger than that of the frame data in the present frame period (see Paragraph 40, Lines 1-7);

if the voltage value of the frame data in the present frame period is smaller than that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is smaller than that of the frame data in the present frame period (see Paragraph 40, Lines 7-11);

if the voltage value of the frame data in the present frame period is equal to that of the frame data in the previous frame period,

the voltage value of the over-drive data voltage pulse is equal to that of the frame data in the present frame period (*see Paragraph 40, Lines 11-15*).

The Applicant contends, "*the cited prior art of Ham also fails to disclose the main technical features of the present invention concerning producing a plurality of corresponding delayed frame data by delaying the plural frame data and the way of deciding the voltage value of an over-drive data voltage pulse mentioned above*" (see Page 10 of the Response filed on 7 October 2009). However, the examiner respectfully disagrees.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's arguments with respect to *claims 13-23* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The documents listed on the attached '*Notice of References Cited*' are cited to further evidence the state of the art pertaining to driving liquid crystal displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
9 February 2010